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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,416	07/09/2001	Guoqiang Xing	TI-31729	7364

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER

NGUYEN, THANH T

ART UNIT PAPER NUMBER

2813

DATE MAILED: 03/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/901,416

Applicant(s)

XING ET AL.

Examiner

Thanh T. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 December 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 12/16/02 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-13 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Flanner et al. (U.S. Patent No. 6,410,437) in view of Blossie et al. (U.S. Patent No. 6,399,512).

Regarding to claims 1-4, Flanner et al. teaches in figures 3-12 a method of forming interconnects comprising:

providing a silicon substrate (16) containing one or more electrically conductive devices (18),

forming a first dielectric layer (14) over the silicon substrate (16),

forming a second dielectric layer (8, 12, an OSG as claimed in claim 2, layer (10) is an optional layer therefore dielectric layer (8, and 12) are formed as a single unitary layer (see col.

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5, lines 20-26)) over first dielectric layer (14), the dielectric constant of second dielectric layer is less than 3.0 (as claimed in claim 1, see col. 1, lines 28-47, organosilicate glass (OSG) low-k material dielectric constant is lower than 4.0),

forming a first hardmask layer (6, a silicon nitride (inorganic) cap layer is used as a masking layer to etch a trench (20) as shown in figures 7-8, as claimed in claim 4) over the second dielectric layer (8, 12, OSG),

forming a second mask layer (4, antireflective layer is used as a masking layer to etch a trench 20 as shown in figures 7-8) on the first hardmask layer (6),

Forming a trench (20) in the second dielectric layer (8, 12), and

Filling the trench with a conductive material (copper, see col. 8, lines 28-29, as claimed in claim 3).

Flanner teaches using an anti-reflective layer (4) as a mask to etch a trench (20) in second dielectric layer (8, 12) as shown in figures 7-8, but fails to teach that an antireflective layer is a hardmask layer (non-organic material) comprises a titanium nitride layer (TiN). Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Blossé et al. Blossé et al. teaches a method of forming a contact trench structure by using an antireflective layer of TiN as a mask layer (see col. 5, lines 50-67). Since, TiN is an inorganic material (not an organic material, such as photoresist), hence TiN is a hardmask layer.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have used a TiN as a second hardmask layer in the process of Flanner et al. as taught by Blossé et al. *because* TiN layer is not only functioning as a masking layer to protect the underlying layer during trench etching but also having antireflection property

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during photolithographic process so that a greater resolution in photolithographic process to produce a contact trench structure for interconnects can be obtained.

Regarding to claims 5-8, Flanner teaches in figures 9-14 a method for forming interconnects comprising:

providing a silicon substrate (16) containing one or more electrically conductive devices (18),

forming a first dielectric layer (14) over the silicon substrate (16),

forming a second dielectric layer (8, 12, an OSG as claimed in claim 6, layer (10) is an optional layer, therefore dielectric layer (8, and 12) are formed as a single unitary layer (see col. 5, lines 20-26)) over first dielectric layer (14), the dielectric constant of second dielectric layer is less than 3.0 (as claimed in claim 5, see col. 1, lines 28-47, organosilicate glass (OSG) low-k material dielectric constant is lower than 4.0),

forming a first hardmask layer (6, a silicon nitride (inorganic) cap layer is used as a masking layer to etch a trench 20 as shown in figures 7-8, as claimed in claim 8) over the second dielectric layer (8, 12, OSG),

forming a second mask layer (4, antireflective layer is used as a masking layer to etch a trench 20 as shown in figure 10) on the first hardmask layer (6),

Etching a first opening in the second mask layer (4) of a first width (see figure 10),

Forming a first trench of a second width (see figure 10) in the second dielectric layer (8, and 12), the second width is less than the first width (see figure 10),

Etching a second opening in the first hardmask layer (6) of a first width (see figure 11),

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Forming a second trench of a first width in the second dielectric layer (8, 12), the second trench is positioned over the first trench (see figure 12, noted that layer 8 and 12 are formed as a single unitary layer), and

Filling first and second trenches with a conducting material (copper, see col. 8, lines 28-29, as claimed in claim 7).

Flanner teaches using an anti-reflective layer (4) as a mask to etch a trench (20) in second dielectric layer (8, 12) as shown in figures 9-10 but fails to teach that an antireflective layer is a hardmask layer (non-organic material) comprises a Titanium nitride layer (TiN). Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Blosse et al. Blosse et al. teaches a method of forming a contact trench structure by using an antireflective layer of TiN as a mask layer (see col. 5, lines 50-67). Since, TiN is an inorganic material (not an organic material, such as photoresist), hence TiN is a hardmask layer.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have used a TiN as a second hardmask layer in the process of Flanner et al. as taught by Blosse et al. *because* TiN layer is not only functioning as a masking layer to protect the underlying layer during trench etching but also having antireflection property during photolithographic process so that a greater resolution in photolithographic process to produce a contact trench structure for interconnects can be obtained.

Regarding to claims 9-13, Flanner teaches in figures 9-14, a method for forming interconnects, comprising:

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providing a silicon substrate (16) containing one or more electrically conductive devices (18),

Forming a first etch stop layer (14) over the silicon layer (16),

Forming a first dielectric layer (12, OSG as claimed in claim 10) over the first etch stop layer (14), the dielectric constant of the first dielectric layer is less than 3.0 (as claimed in claim 9, see col. 1, lines 28-47, organosilicate glass (OSG) low-k material dielectric constant is lower than 4.0),

Forming a second etch stop layer (10) over the first dielectric layer (12),

Forming a second dielectric layer (8, OSG as claimed in claim 11) over the second etch stop layer (10), dielectric constant of second dielectric layer is less than 3.0 (as claimed in claim 9, see col. 1, lines 28-47, organosilicate glass (OSG) low-k material dielectric constant is lower than 4.0),

forming a first hardmask layer (6, a silicon nitride (inorganic) cap layer is used as a masking layer to etch a trench 20 as shown in figures 7-8, as claimed in claim 13) over the second dielectric layer (8),

forming a second mask layer (4, antireflective layer is used as a masking layer to etch a trench 20 as shown in figure 10) on the first hardmask layer (6),

Etching a first opening in the second hardmask layer (4) of a first width (see figure 10),

Forming a first trench of a second width in the second dielectric layer (8), the second width is less than the first width (see figure 10),

Etching a second opening in the first hardmask layer (6) of a first width (see figure 11),

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Forming a second trench of a first width in the second dielectric layer (8), second trench is positioned over the first trench (see figure 12),

Simultaneously etching second trench to a depth of the second etch stop layer (10) and first trench to a depth of the first etch stop layer (see figure 12), and

Filling the first and second trenches with a conducting material (copper, see col. 8, lines 28-29, as claimed in claim 12).

Flanner teaches using an anti-reflective layer (4) as a mask to etch a trench (20) in second dielectric layer (8, 12) as shown in figures 9-10 but fails to teach that an antireflective layer is a hardmask layer (non-organic material) comprises a Titanium nitride layer (TiN). Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Blossé et al. Blossé et al. teaches a method of forming a contact trench structure by using an antireflective layer of TiN as a mask layer (see col. 5, lines 50-67). Since, TiN is an inorganic material (not an organic material, such as photoresist), hence TiN is a hardmask layer.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have used a TiN as a second hardmask layer in the process of Flanner et al. as taught by Blossé et al. *because* TiN layer is not only functioning as a masking layer to protect the underlying layer during trench etching but also having antireflection property during photolithographic process so that a greater resolution in photolithographic process to produce a contact trench structure for interconnects can be obtained.

Response to Arguments

Applicant's arguments filed 12/16/02 have been fully considered but they are not persuasive.

Applicant contends that Flanner et al. does not teach layers 4 and 6 functions as a hardmask. In response to applicant that Flanner et al. teaches layer 4 and 6 function as hardmask to form the opening (see figure 3-8). Flanner et al teaches layer 4 uses as a mask layer to etch layer 6 (see figure 5), and layer 6 uses as a mask layer to etch layers 8-14 (see figure 6).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

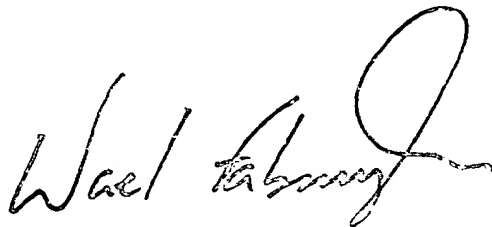
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (703) 308-9439, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:30AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (703) 308-4940. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (See **MPEP 203.08**).

Thanh Nguyen



SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2600